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501.26244CC7

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: MURATA, et al.

Serial No.: 09/998,654

Filed: December 3, 2001

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE  
HAVING SWITCHING MISFET AND CAPACITOR  
ELEMENT AND METHOD OF PRODUCING THE SAME,  
INCLUDING WIRING THEREFOR AND METHOD OF  
PRODUCING SUCH WIRING

AMENDMENT

Assistant Commissioner for Patents  
Washington, D.C. 20231

March 4, 2002

Sir:

In response to the Notice to File Corrected Application Papers mailed  
January 4, 2002, please amend the above-identified application as follows:

IN THE SPECIFICATION

Please delete the present Abstract in its entirety, and substitute therefor the  
enclosed new Abstract, set forth on the page entitled "APPENDIX".

## REMARKS

The Notice mailed January 4, 2002, in connection with the above-identified application, is noted. This Notice required a new Abstract "not to exceed 150 words in length, commencing on a separate sheet". Pursuant thereto, by the present amendments the original Abstract has been deleted, and a new Abstract substituted therefor, which is fewer than 150 words, is in a single paragraph, and reflects the subject matter of the present claims. In view of the presently submitted Abstract, it is respectfully submitted that the requirement for an Abstract in the aforementioned Notice mailed January 4, 2002, has been satisfied.

Attached hereto is a marked-up version of the changes made to the specification by the current Amendment. This marked-up version is on the attached pages, the first page of which is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE".

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing

of this paper, including extension of time fees, to the Deposit Account No. 01-2135  
(Case No. 501.26244CC7) and please credit any excess fees to such Deposit  
Account.

Respectfully submitted,

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WIS/slk

~~$0 < x < 2$ , is used as a protective layer, for an aluminum wiring containing an added element (e.g., Cu) to prevent migration.~~

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ABSTRACT OF THE DISCLOSURE

*method of manufacturing a*  
A semiconductor integrated circuit device having a switching

MISFET<sup>a</sup> and a capacitor element formed over ~~the~~<sup>a</sup> semiconductor substrate, such as a DRAM, is disclosed. ~~In a first aspect of the present invention, the impurity concentration of the semiconductor region of the switching MISFET to which the capacitor element is connected is less than the impurity concentration of semiconductor regions of MISFETs of peripheral circuitry. In a second aspect, the Y-select signal line overlaps the lower electrode layer of the capacitor element. In a third aspect, a potential barrier layer, provided at least under the semiconductor region of the switching MISFET to which the capacitor element is connected,, is formed by diffusion of an impurity for a channel stopper region. In a fourth aspect, the dielectric film of the capacitor element is~~ <sup>formed to be</sup> co-extensive with the capacitor electrode layer over it. ~~In a fifth aspect, the capacitor dielectric film is a silicon nitride film having a silicon oxide layer thereon, the silicon oxide layer being formed by oxidizing a surface layer of the silicon nitride under high pressure. In sixth and seventh aspects, wiring is provided. In the sixth aspect, an aluminum wiring layer and a protective (and/or barrier) layer are formed by sputtering in the same vacuum sputtering chamber without breaking the vacuum between forming the layers; in the seventh aspect, a refractory metal, or a refractory metal silicide  $QSi_x$ , where Q is a refractory metal and~~

*The upper electrode of the capacitor element is formed to be larger than the lower electrodes.*